Article of 1999[1] to Wang et al. [hereinafter "Wang"]. Claims 7 and 8 stand rejected under the same as being unpatentable over Takeuchi in view of Yamada and in further view of U.S. Patent No. 5,374,847 to Araki et al. [hereinafter "Araki"]. Claims 9, 10 and 14 stand rejected under the same as being unpatentable over Takeuchi in view of Klein and in further view of Araki. Claims 13, 15 and 18 stand rejected under the same as being unpatentable over Takeuchi in view of Klein and in further view of Araki and U.S. Patent No. 5,793,081 to Tomioka et al. [hereinafter "Tomioka"].

By this amendment claim 5 has been amended to address the Examiner's concerns and the remainder of the claims have been amended to correct minor informalities. Thus, claims 1-18 are presently pending in this application for consideration.

Applicant respectfully submits that claims 1-18 are patentably distinguishable over the cited references as required by § 103. Applicant further submits that none of the cited references, whether considered alone or in combination, discloses, suggests, or teaches (1) a silicon nitride layer having a low trap density as recited in independent claims 1 and 9 and (2) a silicon nitride layer having a low hydrogen density as recited in independent claims 7 and 14. Thus, these independent claims, as well as claims dependent therefrom, are allowable over the cited references. This distinction will be further described in the following sections.

THE CLAIMS ARE IN PROPER FORM

Claims 5, 6, 11, 12, 16 and 17 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. While Applicant is of the opinion that the claims are in fact definite, Applicant has amended the claims for further clarity and as suggested by the Examiner with the following exceptions.

With respect to claims 11-12 and 16-17, Applicant respectfully submits that the feature of a double-layered silicon nitride layer being contiguous to both a floating gate and a control gate

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[1] Applicant respectfully submits that the Examiner has not established that this reference can be properly used as prior art against the claims in the present application. The present application has a filing date of December 8, 1999. The cited reference merely indicates a copyright date of 1999. Thus, it cannot be established that the cited reference was printed or made available prior to the filing of the present application and therefore fails to qualify as prior art.

recited in independent claims 9 and 14 is consistent with the feature of a silicon oxide layer being contiguous to at least the floating gate and the control gate. As shown in FIG. 3A and described on pages 10, lines 12-20 of the present specification, a third embodiment of the present invention discloses a double-layered silicon nitride layer. With this alternative arrangement, the silicon oxide layer is interposed between the nitride layers. Thus, the nitride layers are contiguous with both the floating gate and the control gate. This arrangement is not inconsistent with independent claims 9 and 14. Each of these claims states that the silicon oxide layer is contiguous with at least one of the floating gate and the control gate. With the addition of another silicon nitride layer, the silicon oxide layer is no longer contiguous with the floating gate and the control gate.

Accordingly, Applicant respectfully submits that the claims are definite and satisfy the requirements set forth under 35 U.S.C. § 112, second paragraph. Withdrawal of this rejection is thus, respectfully requested.

THE CLAIMS ARE PATENTABLE OVER THE CITED REFERENCES

The present invention is directed to a non-volatile semiconductor memory cell having a stacked gate structure. A conventional stacked gate structure shown in FIG. 4A includes an insulating layer 2, provided on a p-type silicon substrate 1. The stacked gate structure further includes a floating gate 4 provided through a tunnel insulating layer 3 and an Oxide-Nitride-Oxide (ONO) layer 5 as an inter-layer insulating layer. The inter-layer insulating layer includes a silicon oxide layer 5a, a silicon nitride layer 5b and a silicon oxide layer 5c, respectively. Also, a control gate 6 is provided on the ONO layer 5. Each of the silicon oxide layers requires a thickness of 5-6nm for preventing electric charges from leaking out during a writing operation of the memory cell and the silicon nitride layer requires a thickness of about 10nm. Thus, the thickness of the ONO layer 5 is approximately, 15-16nm. There are, however, several drawbacks with the conventional stacked gate structure.

One drawback is the difficulty in reducing the size of the ONO layer to approximately a thickness of about 14nm in order to operate the memory cell at a low voltage and provide a large capacitance between the floating gate and the control gate. This is difficult to achieve with the ONO layer of the conventional stacked gate structure.

Another drawback is the formation of a gap called a "bird's beak" formed between the floating gate 4 and the control gate 6. The bird's beak decreases the capacitance coupling between the floating gate 4 and the control gate 6. This typically occurs when the silicon oxide layer 5a is provided by a Chemical Vapor Deposition (CVD).

One advantage of the present invention is that there is a large capacitance coupling between a control gate and a floating gate while securing an electric field relieving effect and preventing electric charges from leaking. This is accomplished by providing (1) a silicon nitride layer having a low trap density as recited in independent claims 1 and 9 and (2) a silicon nitride layer having a low hydrogen density as recited in independent claims 7 and 14. According to one embodiment of the present invention, the first silicon nitride layer is provided by either the CVD or a Low Pressure Chemical Vapor Deposition (LPCVD) while the second silicon nitride layer is provided by a Jet Vapor Deposition (JVD) method. Thus, the second silicon nitride layer is lower in trap level density than the first silicon layer and has a weaker leak current. The cited references fail to disclose these features.

As a preliminary matter, the Takeuchi patent is directed to a stacked non-volatile semiconductor memory having a Nitride-Oxide-Nitride (NON) layered structure. This structure is completely different from the structure disclosed in the present application. While the Takeuchi patent, describes in its background section a conventional stacked non-volatile semiconductor memory having an ONO layered structure including having a floating gate, a control gate and an inter-insulating layer, this conventional structure suffers from the same drawbacks and disadvantages discussed above. Takeuchi fails to disclose and the Examiner correctly notes, a silicon nitride layer having a quantity of hydrogen content of $10^{19}/cm^3$ or less and a silicon nitride layer with a low trap density. The Examiner relies on the Klein, Yamada and Wang references to cure these deficiencies.

The Klein reference discloses material and processes for use in flat panel displays. These materials and processes operate at low temperatures compatible with transparent plastics. The method for depositing the silicon nitride employed by the Klein reference is a Plasma Enhanced Chemical Vapor Deposition (PECVD) method. The Klein reference further discloses creating films with an atomic hydrogen concentration near 20% at 50 degrees Celsius.

The Klein reference also fails to disclose the claimed features of a silicon nitride layer having a quantity of hydrogen content of $10^{19}/cm^3$ or less and a silicon nitride layer with a low

trap density. First, the PECVD method disclosed in Klein is not the same as the CVD, LPCVD and JVD disclosed in the present application. Each of these deposit methods has different advantages and applications and creates unique characteristics in the silicon nitrate. For example, silicon nitride formed by the CVD method has a higher hydrogen density than that found by the LPCVD method and has a higher layer forming rate. Moreover, the Examiner has failed to provide any factual basis for the assertion that the trap density is proportional to the hydrogen content. Thus the claimed features of a silicon nitride layer having a quantity of hydrogen content or $10^{19}/cm^3$ or less and a silicon nitride layer with a low trap density have not been met by the Klein reference whether considered alone or in combination with Takeuchi.

In addition, Applicant respectfully submits that care must be taken so that the application at issue is not used as a guide to combine pieces of earlier devices to reach a conclusion of obviousness. See Lindemann Maschinefabrik GMBH v. American Hoist and Derrick Co., 730 F.2d 1452, 1462 (Fed. Cir. 1984) (requiring the prior art to suggest the desirability to combine the references). Indeed, the requirement of some motivation to combine references is a safeguard against the use of impermissible hindsight. Nothing in the references suggests they should be combined in the manner suggested by the Examiner. In particular, nothing in the references suggests combining a NON film created using a CVD method with a silicon nitride film formed using a PECVD method. As stated above, each of these deposition methods has different advantages and creates different results in the silicon nitride. Thus, one of ordinary skill in the art would not combine these reference in the manner suggested by the Examiner to arrive at the claimed invention because these references relate to different structures and describe different methods in creating these structures.

The Yamada reference is written the Japanese language. Thus, this reference is limited to the translated Abstract, Constitution and the drawings. The Yamada reference is directed to a non-volatile memory preventing leakage current to a gate electrode. This is accomplished by capturing electric charges in a silicon oxide layer/silicon nitride layer through a tunnel effect. According the Yamada, a second silicon nitride layer is disposed on a first silicon nitride layer using a plasma DVD method. The Yamada reference differs from the invention disclosed in the present application in that the method of depositing Yamada's second silicon nitride layer is by a plasma DVD method. Moreover, the Yamada reference also fails to disclose each of the claimed features recited in the independent claims.

In the Wang reference, which has not been properly established as prior art, a method for fabricating a silicon nitride film is disclosed. The silicon nitride layer is generated using the PECVD method. Wang also fails to disclose the claimed features of a silicon nitride layer having a quantity of hydrogen content of $10^{19}/cm^3$ or less and a silicon nitride layer with a low trap density. Again, there is no support for the Examiner's allegations that the trap density is proportional to the hydrogen content.

The Araki reference discloses a non-volatile semiconductor memory device having a passivation film. According to Araki, a memory cell is formed in the main surface area of a semiconductor substrate with an inter-level insulation film formed on the substrate to cover the memory cell. The objective of the invention disclosed in Araki is to provide the passivation film formed of material that contains at least silicon and oxygen and whose refractive index is set to be not less the 1.48 and not more that 1.65. Nothing in Araki discloses or suggests the claimed features of a silicon nitride layer having a quantity of hydrogen content of $10^{19}/cm^3$ or less and a silicon nitride layer with a low trap density.

Therefore, even assuming arguendo that the cited references were properly combinable, the resulting combination would not result in each of the features of the presently pending claims.

In view of the comments above, it is respectfully submitted that the cited references do not render obvious the subject matter recited in independent claims 1, 7, 9 and 14. Moreover, since independent claims 1, 5, 7, 9 and 14 are allowable, the claims dependent therefrom, namely claims 2-4, 6, 8, 10-13 and 15-18 are also allowable. Further remarks regarding the asserted relationship between the claims and the cited references are not necessary, in view of their allowability. The Applicant's silence as to the Examiner's comments is not indicative of an acquiescence to the stated grounds of rejection.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance,

the Examiner is requested to call the undersigned attorney at the Washington, D.C. telephone number 202 637-3615 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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Version with markings to show changes made:

IN THE SPECIFICATION:

Changes to page 1, line 19.

FIGS. 4A and 4B show sections, taken in two directions orthogonal to each other, of the memory cell structure described above. Normally in a flash memory, the control gate of [the] a plurality of memory cells are consecutively arranged and serve as word lines. FIG. 4A is the section in the direction parallel to a direction of the word line.

Changes to page 2, line 10.

[Te] The silicon oxide layer 5a, on the side of the floating gate 4, of the ONO layer 5, if a layer thickness thereof is 5 – 6nm, works as a Fowler-Nordheim type tunnel current conductive mechanism, wherein the electric current flowing with a low electric field is extremely small. Further, a barrier height of the silicon oxide layer 5a with respect to silicon is as high as 3.2 eV. Accordingly, if the silicon oxide layer 5 has no [defect] defects and there is no electric field enhancement effect based on a two-dimensional configuration of the floating gate 4, only the silicon oxide layer 5a must be capable of sufficiently retaining the electrons for a long time. In fact, however, there exist [the defect] defects and the two-dimensional electric field enhancement effect, and hence the ONO layer is used.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Once Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on [said] the semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on [said] the floating gate,

wherein [said] the inter-insulating layer includes:

a silicon oxide layer contiguous to [said] the floating gate;

a first silicon nitride layer provided by a CVD method on [said] the silicon oxide layer; and

a second silicon nitride layer provided on [said] the first silicon nitride layer and having a lower trap density than that of said [first] the silicon nitride layer.

2. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 1, wherein [said] the second silicon nitride layer is formed by carrying, over a surface of [said] the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

3. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of [said] the first silicon nitride layer is $10^{21}/cm^3$ or more.

4. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 1, wherein a quantity of hydrogen content of [said] the second silicon nitride layer is $10^{19}/cm^3$ or more.

5. (Once Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on [said] the semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on [said] the floating gate,

wherein [said] the inter-insulating layer comprises:

a silicon oxide layer contiguous to [said] the floating gate and formed by a CVD method; and

a silicon nitrate layer deposited on [said] the silicon oxide layer [and], the silicon oxide layer having a lower trap density than that of the silicon nitride layer[formed by a CVD method].

6. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 5, wherein [said] the silicon oxide layer is deposited by carrying, over a surface of [said] the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

7. (Once Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on [said] the semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on [said] the floating gate,

wherein [said] the inter-insulating layer includes:

a silicon oxide layer contiguous to [said] the floating gate; and

a silicon oxide layer deposited on [said] the silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

8. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 7, wherein [said] the silicon oxide layer is deposited by carrying, over a surface of [said] the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

9. (Once Amended) A volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory having a floating gate provided through a tunnel insulating layer on [said] the semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on [said] the floating gate,

wherein [said] the inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of [said] the floating gate and [said] the control gate, and having a lower trap density than that of a silicon nitride layer formed by a CVD method.

10. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 9, wherein [said] the silicon nitride layer is formed by carrying, over a surface of [said] the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

11. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 9, wherein [said] the silicon nitride layers are so double-layered as to be contiguous to both of [said] the floating gate and [said] the control gate, and

a silicon oxide layer is interposed in between [said] the double-layered silicon nitride layers.

12. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 9, wherein [said] the silicon nitride layers are so double-layered as to be contiguous to both of [said] the floating gate and [said] the control gate, and

A stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between [said] the double-layered silicon nitride layers.

13. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 9, wherein [said] the silicon nitride layer is provided only on the side contiguous to [said] the floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are foamed by the CVD method, are provided on [said] the silicon nitride layer.

14. (Once Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on [said] the semiconductor substrate, and a control gate provided through an inter-layer [insulting] insulating layer on said floating gate,

wherein [said] the inter-insulating layer includes:

a silicon oxide layer serving as a layer contiguous to at least one of [said] the floating gate and [said] the control gate, and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

15. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 14, wherein [said] the silicon nitride layer is formed by carrying, over a surface of [said] the substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

16. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 14, wherein [said] the silicon nitride layers are so double-layered as to be contiguous to both of [said] the floating gate and said control gate, and

a silicon oxide layer is interposed in between [said] the double-layered silicon nitride layers.

17. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 14, wherein [said] the silicon nitride layers are so double-layered as to be contiguous to both of [said] the floating gate and [said] the control gate, and

a stacked layer consisting of a silicon oxide layer and a silicon nitride layer formed by a CVD method is interposed in between [said] the double-layered silicon nitride layers.

18. (Once Amended) [A] The non-volatile semiconductor memory device according to claim 14, wherein [said] the silicon nitride layer is provided only on the side contiguous to [said] the floating gate, and

a silicon oxide layer and a stacked layer consisting of a silicon nitride layer and a silicon oxide layer which are formed by the CVD method, are provided on [said] the silicon nitride layer.